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| 09/773,164 | 01/31/2001 | Carsten Noeske | Micronas.5873 | 6108 |

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| EXAMINER | |
|---|---|
| DO, CHAT C | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/773,164 | NOESKE, CARSTEN | |
| | Examiner | Art Unit | |
| | Chat C. Do | 2193 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This communication is responsive to Amendment filed 05/11/2007.

2. Claims 1-11 and 19-24 are pending in this application. Claims 1, 7, and 19 are independent claims. In Amendment, claims 12-18 are cancelled and claims 19-24 are newly added. This Office Action is made final.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-10, 19-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deutsch et al. (U.S. 4,031,377).

Re claim 1, Deutsch et al. disclose in Figure 1 a computing device on a monolithic integrated circuit for multiplying together a digitized multiplier signal value (e.g. C or output of 82) and a digitized multiplicand signal value (e.g. S or output of 81), computing device comprising: an input interface (e.g. component 81) that receives multiplicand and provides a received multiplicand indicative thereof (e.g. component 80); a first place shifting device (e.g. component 13) that includes a first logical assignment circuit to shift data bits of received multiplicand in response to a first shift command

signal (e.g. components 17-21), and provides a first shifted signal indicative thereof (e.g. component 26); a second place shifting device (e.g. component 12) that includes a second logical assignment circuit to shift data bits of received multiplicand in response to a second shift command signal (e.g. component 16), and provides a second shifted signal indicative thereof (e.g. component 25); means for summing (e.g. component 27) first and second shifted signals (e.g. components A and B) to provide a summed signal value that is indicative of the product of multiplier signal value and multiplicand value (e.g. component 28' and col. 9 line 60 to col. 10 line 2); and a control device (e.g. component 14) that receives a signal indicative of multiplier (e.g. component 15), and generates (e.g. col. 2 lines 5-15, col. 2 lines 25-29, and col. 9 lines 3-9), first (e.g. component 16) and second shift command signals (e.g. components 18-21) indicative of multiplier value.

Deutsch et al. do not disclose in Figure 1 the first and second means are bi-directionally shifter. However, Deutsch et al. discloses another embodiment the shift circuit would be a bi-directional shifter for either shifting left or right depending on the multiplier factor (e.g. col. 4 lines 5-12).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the mono-directional shift circuits with the bi-directional shift circuits with functional as cited in Deutsch et al.'s alternative embodiment because it would enable to correctly multiplying with decimal factor (e.g. col. 9 line 60 to col. 10 line 2).

Re claim 2, Deutsch et al. further disclose in Figure 1 a memory device for storing summed signal, and for providing past values of summed signal value (e.g. component 83).

Re claim 3, Deutsch et al. further disclose in Figure 1 means for summing receives and sums a signal value from memory device indicative of a past value of summed signal value with first and second shifted signals to provide summed signal value (e.g. component 83 acts as an accumulator to sum all the terms).

Re claim 4, Deutsch et al. further disclose in Figure 1 first place shifting device (e.g. component 13) comprises a first sign inverter (e.g. component table III in col. 6) that receives and selectively inverts the sign of received multiplicand (e.g. component S) to provide a second sign inverted received multiplicand signal that is input to first logical assignment circuit (e.g. component 13) for bit shifting (e.g. col. 5 lines 10-15 and table III in col. 6).

Re claim 6, Deutsch et al. further disclose in Figure 1 control unit (e.g. component 14) generates a first sign inversion command signal (e.g. components 17-19) in response to multiplier value, wherein first sign inversion signal is input to first sign inverter to selectively enable the sign inversion (e.g. table III in col. 6).

Re claim 7, Deutsch et al. disclose in Figure 1 a monolithic integrated circuit on a monolithic integrated circuit for multiplying together a digitized multiplier signal value and a digitized multiplicand signal value (e.g. abstract wherein multiplier signal value and multiplicand signal value would be 82 and 81 respectively), computing device comprising: an input interface (e.g. components 81 and 82) that receives multiplicand and

provides a received multiplicand indicative thereof, first means (e.g. component 12) for shifting data bits of received multiplicand in response to a first shift command signal, and for providing a first shifted signal indicative thereof; second means (e.g. component 13) for shifting data bits of received multiplicand in response to a second shift command signal, and for providing a second shifted signal indicative thereof, means (e.g. component 27) for summing first and second shifted signals to provide a summed signal value that is indicative of the product of multiplier and multiplicand (e.g. output of 28 as X = SC); and a control device (e.g. component 14) that receives a signal indicative of multiplier that is a binary coded number using canonical form, and generates, within at least a clock cycle (e.g. col. 2 lines 5-15, col. 2 lines 25-29, and col. 9 lines 3-9), first and second shift command signals (e.g. components 16 and 17-21) indicative of multiplier value.

Deutsch et al. do not disclose in Figure 1 the first and second means are bi-directionally shifter. However, Deutsch et al. discloses another embodiment the shift circuit would be a bi-directional shifter for either shifting left or right depending on the multiplier factor (e.g. col. 4 lines 5-12).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the mono-directional shift circuits with the bi-directional shift circuits with functional as cited in Deutsch et al.'s alternative embodiment because it would enable to correctly multiplying with decimal factor (e.g. col. 9 line 60 to col. 10 line 2).

Re claim 8, it is a means claim of claim 2. Thus, claim 8 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 9, it is a means claim of claim 3. Thus, claim 9 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 10, it is a means claim of claim 4. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 19, it has similar limitations cited in claim 1. Thus, claim 19 is also rejected under the same rationale as cited in rejection of rejected claim 1.

Re claim 20, it has similar limitations cited in claim 2. Thus, claim 20 is also rejected under the same rationale as cited in rejection of rejected claim 2.

Re claim 21, it has similar limitations cited in claim 3. Thus, claim 21 is also rejected under the same rationale as cited in rejection of rejected claim 3.

Re claim 22, it has similar limitations cited in claim 4. Thus, claim 22 is also rejected under the same rationale as cited in rejection of rejected claim 4.

Re claim 24, it has similar limitations cited in claim 6. Thus, claim 24 is also rejected under the same rationale as cited in rejection of rejected claim 6.

5. Claims 5, 11, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deutsch et al. (U.S. 4,031,377), as applied to claim 4 above, in view of Main (U.S. 5,402,369).

Re claim 5, Deutsch et al. do not disclose in Figure 1 a second place shifting device comprises a second sign inverter that receives and inverts the sign of received multiplicand to provide a sign inverted received multiplicand signal that is input to

second logical assignment circuit for bit shifting. However, Main discloses in Figure 1 that the multiplier can be factored as multiple plus or minus terms in col. 5 lines 10-15.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add an inverter in the first place shifting device as seen in Main's reference into Deutsch et al.'s reference because it would enable to compute the product faster and more efficient (e.g. without the first inverter, the system has to bypass the first place shifting device and subtract in the next clock using the second place shifting device).

Re claim 11, it is a means claim of claim 5. Thus, claim 11 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 23, it has similar limitations cited in claim 5. Thus, claim 23 is also rejected under the same rationale as cited in rejection of rejected claim 5.

***Response to Arguments***

6. Applicant's arguments filed 05/11/2007 have been fully considered but they are not persuasive.

a. The applicant argues in pages 8-9 for claim 1 that the cited reference fails to disclose the claimed limitations "means for summing said first ...indicative of the product of said multiplier and said multiplicand" since the cited reference by Deutsch discloses the multiplication product only after the right or left shifting circuit 29 in Figure 4.

The examiner respectfully submits that the applicant has not fully considered Figure 1 as the second embodiment as clearly addressed in col. 9 line 60 to col. 10

line 2 wherein the right or left shifting circuit 29 can be place in the front Of the integrated circuit as 29' and the output of adder 27 will yield a multiplication product directly (e.g. {A*B}*C == {C*A}*B).

b. The applicant argues in pages 9-11 for claim 1 that it is not obvious to modify the circuit as suggested to be the same as the claimed invention since the system of Deutsch is particularly configured to arrange to handle the numbers shown in Table II of Deutsch.

The examiner respectfully submits that the claim does not limit to which system of numbers the claimed invention can handle; as long as the found reference cites all the features/limitations within the claims, then the found reference can be used to reject the claimed invention. The only missing element/limitation in the single embodiment of the cited reference is the bi-directionally shifter in place of the left shifter. However, this bi-directional shifter is also taught by the reference as for shifting in both directions. Thus, it is obvious and proper to combine to yield the claimed invention (e.g. see KSR).

c. The applicant argues in pages 11-13 for claim 7 that it is not obvious and improper to modify the ONLY left shift circuit as the bi-directionally shift circuit as cited in the claimed invention.

The examiner respectfully submits that the only missing element/limitation in the single embodiment of the cited reference is the bi-directionally shifter in place of the left shifter. However, this bi-directional shifter is also taught by the reference

as for shifting in both directions. Thus, it is obvious and proper to combine to yield the claimed invention (e.g. see KSR).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,726,926 to Makino discloses a shifter for shifting floating point number utilizing arithmetic operation of redundant binary number, and adder containing the same.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

January 6, 2008